Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) ~~The PLL circuit according to claim 1,~~ A phase-locked loop (PLL) circuit comprising:

a first loop circuit for generating a first clock signal which is synchronized with a first reference signal, wherein the first reference signal is compared with the first clock signal to generate a first control voltage; and

a second loop circuit connected to the first loop circuit for generating a second clock signal which is synchronized with a second reference signal having a frequency which is sufficiently lower than the frequency of the first reference signal, wherein the second reference signal is compared with the second clock signal to generate a second control voltage;

wherein the first loop circuit includes a first voltage controlled oscillator for generating the first clock signal in accordance with the first control voltage;

wherein the second loop circuit includes a second voltage controlled oscillator for generating the second clock signal in accordance with the first control voltage and the second control voltage; and

wherein the first reference signal is a wobble signal of an optical disc, and the second reference signal is a land prepit signal of the optical disc.

3. (Currently Amended) The PLL circuit according to claim [[~~1~~]] 2, wherein the second loop circuit further includes an adder connected to the second voltage controlled

oscillator for generating a sum voltage by adding the first control voltage and the second control voltage.

4. (Currently Amended) A phase-locked loop (PLL) circuit comprising:

a first loop circuit for generating a first clock signal which is synchronized with a first reference signal; and

a second loop circuit connected to the first loop circuit for generating a second clock signal which is synchronized with a second reference signal, wherein the frequency of the second reference signal is lower than the frequency of the first reference signal;

wherein the first loop circuit includes:

a first frequency divider for generating a first divisional clock signal by dividing the first clock signal by a predetermined first frequency dividing ratio;

a first phase comparator connected to the first frequency divider for receiving the first reference signal and the first divisional clock signal and generating a first comparison signal in accordance with the first reference signal and the first divisional clock signal;

a first low-pass filter connected to the first phase comparator for generating a first control voltage corresponding to the first comparison signal; and

a first voltage controlled oscillator connected to the first low-pass filter for generating the first clock signal in accordance with the first control voltage;

wherein the second loop includes:

a second frequency divider for generating a second divisional clock signal by dividing the second clock signal by a predetermined second frequency dividing ratio;

a second phase comparator connected to the second frequency divider for receiving the second reference signal and the second divisional clock signal and generating a second comparison signal in accordance with the second reference signal and the second divisional clock signal;

a second low-pass filter connected to the second phase comparator for generating a second control voltage corresponding to the second comparison signal; and

a second voltage controlled oscillator connected to the first and second low-pass filters for generating the second clock signal in accordance with the first and second control voltages;

wherein the first reference signal is a wobble signal of an optical disc, and the second reference signal is a land prepit signal of the optical disc.

5. (Original) The PLL circuit according to claim 4; wherein the second voltage controlled oscillator includes:

a first input terminal for receiving the first control voltage;

a second input terminal for receiving the second control voltage; and

a ring oscillator connected to the first and second input terminals and driven by differing first and second control currents respectively corresponding to the first and second control voltages.

6. (Original) The PLL circuit according to claim 5, wherein the second voltage controlled oscillator further includes:

a first current control gate corresponding to the first input terminal; and

a second current control gate corresponding to the second input terminal;

wherein a drive current of the first current control gate is greater than a drive current of the second current control gate; and

wherein the first voltage controlled oscillator includes:

a third input terminal for receiving the first control voltage; and

a fourth input terminal for receiving a constant DC voltage.

7. (Original) The PLL circuit according to claim 4, wherein the first phase comparator includes:

a leading edge comparator connected to the first frequency divider for receiving the first reference signal and the first divisional clock signal and generating a leading edge comparison

signal in accordance with the difference between the timing of the leading edge of the first reference signal and the timing of the leading edge of the first divisional clock signal;

a trailing edge comparator connected to the first frequency divider for receiving the first reference signal and the first divisional clock signal and generating a trailing edge comparison signal in accordance with the difference between the timing of the trailing edge of the first reference signal and the timing of the trailing edge of the first divisional clock signal; and

an adder connected to the leading edge comparator and the trailing edge comparator for generating a sum signal by adding the leading edge comparison signal and the trailing edge comparison signal.

8. (Original) The PLL circuit according to claim 7, wherein the second loop circuit further includes:

a charge pump connected to the second phase comparator for generating a charge pump signal that equalizes a charge time and a discharge time when a leading edge of the second divisional clock signal is synchronized with a pulse center of the second reference signal.

9. (Cancelled)

10. (Original) The PLL circuit according to claim 4, wherein the second loop circuit further includes an adder connected to the second voltage controlled oscillator for generating a sum voltage by adding the first control voltage and the second control voltage.

11. (Cancelled)

12. (Currently Amended) ~~The method according to claim 11,~~ A method for generating a clock signal using a first phase-locked loop (PLL) circuit and a second PLL circuit connected to the first PLL circuit, wherein the first PLL circuit includes a first voltage controlled

oscillator, and the second PLL circuit includes a second voltage controlled oscillator, the method comprising the steps of:

generating a first clock signal which is synchronized with a first reference signal; and

generating a second clock signal which is synchronized with a second reference signal, wherein the frequency of the second reference signal is lower than the frequency of the first reference signal;

wherein the step of generating the first clock signal includes:

generating a first control voltage by comparing the first reference signal and the first clock signal; and

generating the first clock signal in accordance with the first control voltage using the first voltage controlled oscillator; and

wherein the step of generating the second clock signal includes;

generating a second control voltage by comparing the second reference signal and the second clock signal; and

generating the second clock signal in accordance with the first control voltage and the second control voltage using the second voltage controlled oscillator; and

wherein the first reference signal is a wobble signal of an optical disc, and the second reference signal is a land prepit signal of the optical disc.

13. (Currently Amended) The method according to claim [[~~11~~]] 12, wherein the method for generating the second clock signal further includes adding the first control voltage and the second control voltage.